

REMARKS

In response to the Final Office Action mailed May 11, 2005, Applicants respectfully request reconsideration. Claims 1-2 and 4-18 were previously pending in this application. Claims 1, 9, and 10 have been amended. New claim 19 has been added. As a result, claims 1-2 and 4-19 are pending for examination, with claims 1, 9, and 10 being independent claims. No new matter has been added.

I. Request for Interview

Initially, Applicant's representatives would like to request a telephone interview with the Examiner to be conducted in advance of any further Office Action that may be issued. The Examiner is requested to contact the undersigned to schedule such an interview. Applicants' representatives appreciate the courtesy of the Examiner in this regard.

II Rejections Under 35 U.S.C. §102

Claims 1, 2, 4, 8-14 and 16-18, including independent claims 1, 9, and 10, were rejected as being anticipated by Tsay et al. (U.S. Patent No. 6,529,237). Independent claim 1 has been amended to clearly distinguish over Tsay. Claim 9 has been amended for clarification, and the rejections of independent claims 9 and 10 are respectfully traversed.

a. Claim 1

As amended, claim 1 recites a pixel gain amplifier circuit comprising an amplifier having an input and an output, an input capacitor onto which input capacitor charge from an input pixel is sampled during a first of first and second time phases, *wherein the input capacitor is functionally coupled to the input of the amplifier during the first and second time phases*, and a feedback capacitor, coupled between the input and the output of the amplifier, that samples a reference voltage during the first time phase and receives charge from the input capacitor during the second time phase.

In contrast, Tsay discloses a circuit 14 (Fig. 2) wherein sampling capacitor 50 is coupled to an input of operational amplifier 68 by switch 72, such that sampling capacitor 50 is not

functionally coupled to the input of the operational amplifier 68 during a sampling phase of the circuit 14 (Fig. 2; Col. 3, lines 30-32; Col. 4, lines 63-67). Indeed, in the circuit 14 of Tsay, the circuit could not function properly if sampling capacitor 50 was coupled to the operational amplifier 68 during the sampling phase. As discussed in Tsay, switches 66 and 72 are used to isolate sampling capacitors 46 and 50 during the sampling phase so that the sampled signals are isolated from operational amplifier 68 until all sampling operations are complete (Col. 4, lines 63-67). In other words, switches 66 and 72 cannot be turned on until switch 38 samples the reset signal onto sampling capacitor 46 at a first time corresponding to shelf 112 of the CCD output, and switch 42 samples the video signal onto sampling capacitor 50 at a later time corresponding to the signal level 118 of the CCD output (Col. 4, lines 63-67; Col. 5, lines 45-48; Fig. 3). When the switches 66 and 72 are turned on, switch 54 is simultaneously turned on, which will place the true differential voltage on nodes 48 and 58 on the negative and positive and negative outputs of the operational amplifier 68 (Col. 4, line 66 – Col. 5, line 5).

In view of the foregoing, it should be appreciated that the circuit 14 in Tsay does not include an input capacitor functionally coupled to the input of the amplifier during a first time phase during which a charge from an input pixel is sampled onto the input capacitor. Furthermore, the circuit 14 in Tsay would be rendered non-functional if this was the case, for the reasons discussed above. Thus, claim 1 patentably distinguishes over Tsay and withdrawal of the rejection of claim 1 under 35 U.S.C. §102 as being anticipated by Tsay is respectfully requested. Claims 2, 4-8, and 17-19 depend from claim 10 and are patentable for at the same reasons as the independent claim.

b. Claim 9

As amended, claim 9 recites a method of amplifying input pixels, comprising steps of sampling an input pixel during a first of first and second time phases, amplifying the sampled input pixel during the second time phase, and controlling a gain of the amplification of the input pixel at the pixel rate in response to a gain control signal comprising information related to a desired gain.

Tsay discloses a programmable gain amplifier that is operable to precondition a CCD output analog signal (Abstract). Feedback capacitors are provided which, in conjunction with the sampling capacitors, define the gain of the amplifier (Col. 2, lines 17-22). Each of the

sampling capacitors has associated therewith a trimming network for varying the overall effective capacitance of the input sampling capacitor. The capacitance, and thereby the gain of the amplifier, is varied in response to a gain signal (Abstract; Col. 7, lines 25-26).

Tsay does not disclose controlling a gain of the amplification of the input pixel *at the pixel rate* in response to a gain control signal comprising information related to a desired gain. Tsay is silent as to how often the gain of the amplifier is controlled and what may trigger a gain change, but provides no suggestion that gain is controlled at the pixel rate. One example of a potential motivation for controlling a gain of amplification at the pixel rate is that it enables a user to compensate for differences in the average signal level between pixels of different colors (described in Applicants' specification at page 2, lines 18-20). There is no indication that the amplifier of Tsay is capable of processing pixels of different colors. It should be appreciated, however, that processing pixels of different colors is just one exemplary purpose for controlling a gain of amplification of an input pixel at the pixel rate, and is provided merely to assist the Examiner in appreciating an application of the present invention and not to limit any of the independent claims to these particular features.

As should be appreciated from the foregoing, claim 9, as amended, patentably distinguishes over Tsay. Accordingly, withdrawal of the rejection of claim 9 under 35 U.S.C. §102 as being anticipated by Tsay is respectfully requested.

c. Claim 10

Claim 10 is directed to a pixel gain amplifier circuit, the circuit comprising an amplifier having an input, an output and a gain, and means for varying the gain of the amplifier from a first gain for a first pixel to a second gain for a second pixel, wherein the first and second gains are determined, at least in part, by an input capacitor and a feedback capacitor.

Tsay does not disclose or suggest means for varying the gain of the amplifier from a first gain for a first pixel to a second gain for a second pixel. As discussed above, Tsay is silent as to how often the gain of the amplifier is controlled and what may trigger a gain change. Furthermore, Tsay provides no suggestion that the gain of the amplifier is changed from a first gain for a first pixel to a second gain for a second pixel.

As should be appreciated from the foregoing, claim 10 patentably distinguishes over Tsay. Accordingly, withdrawal of the rejection of claim 10 under 35 U.S.C. §102 as being

anticipated by Tsay is respectfully requested. Claims 11-12 and 14-16 depend from claim 10 and are patentable for at the same reasons as the independent claim.

III. Claim Rejections Under 35 U.S.C. §103(a)


Claims 5-7 and 15 are rejected under 35 U.S.C. §103(a) as being obvious over Tsay. Claims 5-7 depend from independent claim 1 and are believed to be allowable for at least the same reasons as claim 1. Claim 15 depends from claim 10 and is believed to be allowable for at least the same reasons as claim 10. Accordingly, for the sake of brevity, Applicants believe that it is unnecessary at this time to argue the allowability of claims 5-7 and 15 and reserve the right to specifically address the patentability of this claim in the future, if deemed necessary.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Katsufumi Nakamura et al., Applicants

By: 
Melissa A. Beede, Reg. No. 54,986
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

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